

# Gokulan Ravi

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## EDUCATION

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**Ph.D. in Electrical & Computer Engineering** Jan 2021 - June 2026 (expected)  
Purdue University, West Lafayette, IN, USA GPA: 3.87/4.00  
▷ *Thesis: Scalable Verification of Memory Consistency in Shared-Memory Systems (funded by NSF)*  
▷ *Co-advised by Mithuna Thottethodi and T. N. Vijaykumar*

**B.Tech + M.Tech (Dual Degree) in Computer Science & Engineering** Jul 2015 - May 2020  
Indian Institute of Technology Madras, Chennai, India GPA: 8.23/10.00

## PUBLICATIONS

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**QED: Scalable Verification of Hardware Memory Consistency** [Under Review] [arXiv:2404.03113](https://arxiv.org/abs/2404.03113)  
[Gokulan Ravi](#), Xiaokang Qiu, Mithuna Thottethodi, T. N. Vijaykumar

- Proposed a methodology to verify hardware memory consistency for unbounded programs (prior works limited to bounded verification of  $\leq 7$  instructions)
- Complexity of the proposed approach is independent of, and scalable with, the system size
- Can be used to verify complex, out-of-order-issue processors, not covered by prior works
- Proved that two instructions and two external events (corresponding to instructions in other threads) are sufficient to capture any consistency violation across all models

**QEF: Verifying Memory Consistency in a superscalar out-of-order-issue processor** [Under Review]  
[Gokulan Ravi](#), Xiaokang Qiu, Mithuna Thottethodi, T. N. Vijaykumar

- Used QED's methodology to formally verify BOOMv3 using Jaspergold
- Proposed abstraction techniques to prevent exponential verification complexity of RTL
- Identified three previously unknown bugs in RTL (two violations, one performance bug)
- Verified Apple M1-equivalent BOOMv3 configuration in under 10 days (first unbounded verification of memory consistency in an out-of-order-issue processor)

**Per-Program Compiler Correctness Verification for Weak Memory Models** [In Preparation]  
[Gokulan Ravi](#), Xiaokang Qiu, Mithuna Thottethodi, T. N. Vijaykumar

- Closes the gap in verifying that HLL programs execute correctly on any hardware
- Uses a novel abstract machine that can be used to verify code generation, compiler transformations, and identify synchronization inefficiencies
- Generic abstract machine extensible to GPUs and heterogenous shared-memory (CPU-GPU and GPU-accelerator) systems
- Implemented a verification pipeline in LLVM to verify C++ to RISC-V and PowerPC compilations

## PROFESSIONAL EXPERIENCE

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**Engineering Intern, Ventana Microsystems Inc.** Jul 2023 - Jan 2024

- Worked on the design, verification and performance analysis of the Branch Predictor Unit for Ventana's V2 processor
- Implemented a secondary branch predictor and a novel feature to optimize timing on the critical path
- Wrote temporal assertions that identified bugs of different complexity, increasing assertion coverage and performance
- Crafted tests for isolating performance of predictors for different types of branches, and exercising internal replacement policies

## Graduate Teaching Assistant

Aug 2019 - May 2024

- Purdue University - Operating Systems (Spring '21, '22, '23, '24), Object Oriented Programming (Fall '21), Compilers (Fall '22)
  - Developed an autograder to automate evaluation of programming homeworks for Operating Systems in Spring '23 for a class of 180 students
  - Ported AST-based compiler's codebase from Java to Python for Compilers course
- IIT Madras - Computer System Design (Fall '19), Systems for Deep Learning (Spring '20)
  - Created course content, programming homeworks and project specifications during the first offering of grad-level SysDL course

## SELECTED PROJECTS

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### SHAKTIMAAN: Systolic-array based co-processor for DNN Inference

Jun 2019 - May 2020

*Masters thesis, IIT Madras*

- Led the implementation of a parameterized systolic-array based co-processor in Bluespec
- Interfaced the systolic array with Shakti C-Class, an 5-stage in-order-issue RISC-V processor
- Built an end-to-end working solution with a prototype compiler based on TVM
- Open-source implementation available at <https://github.com/iitm-sysdl/SHAKTIMAAN>

### MOESI Cache Coherence for in-order processor, IIT Madras

May - Jun 2018, Jan - May 2019

*Summer project (Snoop-based protocol), Senior Design project (Directory-based protocol)*

- Modified memory subsystem of a 5-stage RISC-V core to enable multicore extensions
- Designed the finite state machine and implemented the entire cache controller in Bluespec
- Implemented custom Tilelink-Cacheable (TL-C) bus protocol to support P2P transactions for directory-based implementation

### GPU Kernel Optimization for Graph Neural Networks, Purdue University

Jan 2021 - May 2021

- Initial proposal to build custom ASIC aimed at exploiting ultra sparsity of graphs to accelerate GNNs
- Reported that GPUs SpMM is a good fit and no further opportunity remained to be explored

## SKILLS

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**Relevant Courses:** Computer Architecture, Parallel Computer Architecture, GPU Architecture & Programming, Concurrent Programming, Operating Systems, Advanced Compilers, Distributed Systems, Pattern Recognition & Machine Learning, Deep Learning (CNNs)

**Additional Expertise:** Transformer architectures, LLM systems (training, inference, workload characteristics)

**Programming / Scripting Languages:** C/C++ (including OpenMP, MPI and CUDA), Java, Python (PyTorch), Bash, RISC-V Assembly

**HDL:** SystemVerilog, Bluespec SystemVerilog, Chisel, Tcl scripting

**Tools:** Jaspergold, LLVM, gem5

## OTHER ACTIVITIES

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### Member of Artifact Evaluation Committee, MICRO 54

Aug 2021

Reproduced and verified results of one paper in MICRO 54's proceedings

### Head, Web Operations, Shaastra 2018, IIT Madras

Mar 2017 - Jan 2018

- Led a team of 20 to build the software stack of the technical symposium
- Unified different user-facing applications, streamlined internal operations, increased registrations by 80%

### Instructor, Webops Club, Center for Innovation, IIT Madras

May 2017 - Dec 2019

Organized various workshops in web, mobile app and Python development for undergraduates